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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,985	02/22/2002	Reid James Riedlinger	10971429-1	9993

22879 7590 10/04/2004

HEWLETT PACKARD COMPANY  
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FORT COLLINS, CO 80527-2400

EXAMINER

BRAGDON, REGINALD GLENWOOD

ART UNIT PAPER NUMBER

2188

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/080,985	<b>Applicant(s)</b> RIEDLINGER ET AL.	
	<b>Examiner</b> Reginald G. Bragdon	<b>Art Unit</b> 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 13 August 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Double Patenting*

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 17-18 of U.S. Patent 6,539,457 contains every element of claim 19 of the instant application and as such anticipates claim 19 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. *In re Longi*, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); *In re Berg*, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " *ELI LILLY AND COMPANY v BARR LABORATORIES, INC.*, United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

As per claim 19, the limitation of a memory structure that comprises a plurality of address banks corresponds to the limitation of lines 2-3 of claim 18 of the '457 patent. The limitation of "means for queuing" corresponds to the limitation of "a queue for holding address information" of claim 17 of the '457 patent. The limitation of "means for determining" corresponds to the limitation of lines 4-7 of claim 18 of the '457 patent. The limitation of "means for nominating" corresponds to the "means for issuing" in claim 18 of the '457 patent.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

--or--

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 10-14, and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hetherington et al. (5,930,819).

As per claim 1, Hetherington et al. teaches an L2 data cache including 4 address ports ("a plurality of access ports communicatively coupled to said cache memory structure") and 16 banks ("cache memory structure comprising multiple banks"). See figure 5 and column 4, lines 50-52. A memory scheduling window, or MSW 502, is coupled to the tag array and controls access to the L2 cache. All cache memory access that do not hit in the L1 cache will arbitrate

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and create an entry into MSW 502 (see column 11, lines 61-67). The MSW is organized as a plurality of columns, one for each port, with each column including 32 entries and 4 entries in one row are allowed to launch at the same time. See column 12, lines 24-37. The MSW represents the claimed “queue”. A content addressable memory determines inter-row bank conflicts (“circuitry operable to determine bank conflict for pending access requests for said memory structure”). See column 13, lines 64-67. A picker 606 (“circuitry operable to issue...”) is utilized in selecting a row for launching, where the picker is directed to launch one non-conflicting group of accesses every clock cycle. See column 14, lines 22-42.

The picker 606 issues out of order accesses. Hetherington et al. teaches that port 0 is biased such that the access request in the port 0 entry always gains access first. See column 13, lines 55-56. It is taught that when a row comprises multiple accesses and a bank conflict is detected, the picker launches one non-conflicting group of accesses (see column 14, lines 27-31). Assuming the most basic situation where port entry 0 and port entry 1 in a particular row x conflict, then port entry 0 and port entries 2-3 will launch, while port entry 1 will launch on the next cycle. Therefore, entry 1 of row x will be issued out-of-order with the other entries placed in row x.

As per claim 11 and 19, these claims are rejected for the reasons set forth for claim 1, above. It is further noted that (for claim 11), in the example set forth above, entry 3 is newer than the entry for entry 1 and will be launched prior to entry 1.

As per claim 2, Hetherington et al. teaches a bank conflict between at least two entries in a particular row. See column 13, line 64 to column 14, line 6.

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As per claims 3 and 10, Hetherington et al. teaches the MSW, where each column can be thought of as a queue serving a particular port. See column 12, lines 31-33. The CAM unit compares all entries in a row (which are “sibling” entries) one clock cycle after insertion in the MSW. See column 13, lines 64-67.

As per claim 4, Hetherington et al. teaches that conflict is between an issued entry (i.e. entry 0) and a pending entry (entry 1).

As per claim 12, Hetherington et al. teaches nominating all entries in a row that do not conflict (plus one entry that may conflict) for accessing the L2 cache. See the discussion for claims 1 and 11, above.

As per claims 13 and 20, Hetherington et al. teaches that the entries in a particular row that will access the L2 cache (i.e. all non-conflicting entries plus one conflicting entry) will be launched during the same cycle, i.e. in parallel. See column 14, lines 30-31.

As per claim 14, Hetherington et al. teaches that the CAM unit compares all entries in a row one clock cycle after insertion in the MSW. See column 13, lines 64-67.

5. Claims 1-3, 5-9, 11-12, and 14-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Rangan (6,711,654).

As per claims 1 and 19-20, Rangan teaches a cache memory 107 including a bank array 220 (“multiple banks” or “memory structure”) where each bank allows for one access each clock cycle (column 1, lines 21-23). A queue 210 (“means for queuing”) stores each access request for the bank array, and multiple ports from the queue may access the bank array (“plurality of access ports”) simultaneously (“means for issuing”). See column 1, lines 37-41, and column 3, lines 43-50. Rangan teaches conflict detection unit 240 (“circuitry operable to determine a bank

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conflict” or “means for determining”) which detects multiple requests in queue 210 to access the same bank in the bank array. See column 4, lines 21-23. Rangan further teaches that entries in the queue may access the bank array in an out-of-order mode (“circuitry operable to issue at least one access request to said cache memory structure out of the order it was requested, responsive to a determination of said bank conflict” or “means for nominating”). See column 3, lines 47-50.

As per claim 2, Rangan teaches that the bank conflict is between at least two requests. See column 4, lines 21-23.

As per claim 3, Rangan teaches a queue 210 which stores each access request for the bank array. See above for claim 1. Rangan also teaches comparing a new request for entry in the queue to existing queue entries. See column 4, lines 30-32.

As per claims 5 and 8, Rangan teaches a pipeline, where one type of instruction is completed in stage X and another type of instruction is completed in stage X+2 (“a predefined pipeline...having a plurality of stages with one stage for performing a first type of access and a different stage for performing a second type of access”). See column 5, lines 24-29.

As per claim 6, Rangan teaches that the first type of access is a store access and the second type of access is a load access. See column 5, lines 24-29.

As per claim 7, Rangan teaches that the first type of access is a store access and the second type of access is a load (i.e. read) access. See column 5, lines 24-29.

As per claim 9, Rangan teaches comparing a new request with existing (i.e. older) access requests. See column 4, lines 30-32.

As per claim 11, Rangan teaches a cache memory 107 including a bank array 220 where each bank allows for one access each clock cycle (column 1, lines 21-23). A queue 210 stores

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each access request for the bank array (“storing access requests...to a pending request queue”), and multiple ports from the queue may access the bank array. See column 1, lines 37-41, and column 3, lines 43-50. Rangan teaches conflict detection unit 240 which detects multiple requests in queue 210 to access the same bank in the bank array (“determining at least one access request in said pending request queue that has a bank conflict”). See column 4, lines 21-23. Rangan further teaches that entries in the queue may access the bank array in an out-of-order mode (“determining...that does not have a bank conflict). See column 3, lines 47-50. Since an entry in the queue may not issue until after the conflict is resolved (i.e. the older request has issued) and the queue is an out-of-order queue, then a newer entry will bypass the conflicting entry (“nominating...that does not have a bank conflict for issuance...”).

As per claim 12, Rangan teaches issuing multiple requests stored in the queue 210 to the cache over a period of time. See column 3, lines 40-52.

As per claim 14, Rangan teaches comparing a new request for entry in the queue to existing queue entries. See column 4, lines 30-32.

As per claim 15, Rangan teaches a bank conflict with an existing queue entry, which is older than the new entry. See column 4, lines 36-39.

As per claim 16, Rangan teaches that the first type of access is a store access and the second type of access is a load access. See column 5, lines 24-29.

As per claim 17, Rangan teaches a pipeline, where one type of instruction is completed in stage X and another type of instruction is completed in stage X+2 (“a predefined pipeline...having a plurality of stages with one stage for performing a first type of access and a different stage for performing a second type of access”). See column 5, lines 24-29.

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As per claim 18, Rangan teaches that the first type of access is a store access and the second type of access is a load (i.e. read) access. See column 5, lines 24-29.

*Conclusion*

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McGehearty et al. (6,029,225) teaches bank conflict avoidance in a cache memory.

7. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks  
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All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693** (after October 14, 2004, the "INFORMAL" or "DRAFT" FAX number will be 571-273-4204), only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121  
Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

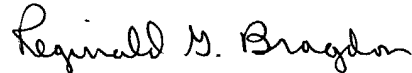
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8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823 (after October 14, 2004, the telephone number will be 571-272-4204). The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903 (after October 14, 2004, the telephone number will be 571-272-4210).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

RGB  
September 30, 2004

  
Reginald G. Bragdon  
Primary Patent Examiner  
Art Unit 2188